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EXAMINER	
WANG, HARRIS C	
ART UNIT	**PAPER NUMBER**
2139	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/755,120	KOBAYASHI, SHINICHIRO	
	Examiner	Art Unit	
	Harris C. Wang	2139	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1.

Claim 1 is pending

Claim 1 has been amended

Response to Arguments

Applicant's arguments filed 8/13/2007 have been fully considered but they are not persuasive.

Applicant argues "Green does not teach or suggest 'a second calculation section performing a second calculation which associates the first address with a second address in one-to one correspondence.' Instead, Greene discloses a hash function 108 that transforms an input key into an address offset that is then added to a base address."

The Examiner responds by referring to page 9 of the first Office Action, where the Examiner cited Greene as teaching 'a second calculation section performing a second calculation which associates the first address with a second address in one-to one correspondence.' The Examiner repeats the same citation where Greene discloses "a second small perfect hash function maps the set of colliding key values to a second output value" (Column 3, lines 60-62). The Examiner interprets the "second small perfect hash function" as the second calculation. The Examiner interprets the

association of the first address with a second address in one-to one correspondence as "map[ping] the set of colliding key values to a second output value."

The Applicant then argues that "Greene does not teach or suggest first or second processing sections that send a **first** address to the N storage sections and that selectively sent a **second** address to the **same** N storage sections. Instead, Greene only discloses sending a **first** address to a **first** memory and a **second** address to a **second** memory."

The Examiner responds by pointing to the cited portion of Greene on Page 9 of the Office Action. ("The memory system 404 can include a first memory portion and a second memory portion." Column 9, lines7-10). The Applicant's arguments suggest that the instant application uses the same memory to store the addresses while Greene stores the first address in a first memory and a second address in a second memory. However because Greene refers to the first memory **portion** and the second memory **portion** as being part of the overall memory system, the Examiner does not believe that the present application is distinguished from Greene.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Greene (6434662).

Regarding Claim 1,

Greene teaches a semiconductor apparatus for storing a key and data, comprising:

N storage sections having first to N-th storage capacities, respectively, the storage sections (where N is an integer greater than one):

storing an externally-input key or data at a received address

and when a key and data are stored at a received address, outputting the key and data; *("it is possible that the search key is not the same as the key stored in the table, but is an "alias" to that key, that just happens to hash to the same bucket. Therefore, even when a single candidate search result is found, the key stored in the table must be compared against the input search key to resolve such aliases" Column 2, lines 7-13). The Examiner interprets that the externally input key is different than the key and data stored at the address. It is inherent that in order to compare the input search key with the candidate search result the stored key and data must be outputted.*

and when a key or data is not stored at a received address, outputting a first signal indicating that a key or data is not stored at the received address, *("the first memory location can be a null entry that includes data indicating that there is no stored data that is associated with the corresponding input key, or with any input key that hashes to that address" Column 4, lines 21-25)*

N comparison sections, the comparison sections:

comparing the externally input key with keys output from the first to N-th storage sections; *("An alias compare is them performed and the stored key value is tested against the input search key (step 214, Column 7, lines 30-35)*

and when the externally input key matches the keys output from the first to N-th storage sections, outputting a second signal indicating that the externally input key matches the keys output from the first to N-th storage sections; externally outputting data output from a storage section which outputs the key that matches the externally input key *(...if they match, associated data can be output (step 216) Column 7, lines 30-35). ("an alias compare is done (step 214) and if there is a match (the address or key is not an alias), then the associated data fetched from the third memory can be output") It is inherent that a signal must be sent before fetching the data from the memory.*

and when the first to N-th storage sections output the first signals, outputting a third signal indicating that the first to N-th storage sections

output the first signals, in key-and-data writing into the first to N-th storage sections; (*...if not, "no match" is output (step 210) based on the failed alias test" Column 7, lines 30-35). The Examiner interprets "no match" as the third signal.*

a first calculation section performing a first calculation which associates the externally input key with a first address in many-to-one correspondence; *("A first hashing function maps the input key values into first output values. The number of first output values is smaller than the number of all possible key values." Column 3, lines 55-57) ("The memory system 404 can include a first memory portion and a second memory portion. First memory portion 416 can include a number of entries that can be accessed according to address values generated by the first hash function calculator" Column 9, lines 7-10)*

a second calculation section performing a second calculation which associates the first address with a second address in one-to-one correspondence; *("a second small perfect hash function maps the set of colliding key values to second output values" Column 3, lines 60-62) ("Second memory portion 418 can include a number of entries that can be accessed according to address values that include outputs from the second hash function calculator 412" Column 9, lines 11-14)*

a first processing section operating when a key and data are written, the first processing section: *("Processing system 402 can include a number of structures, such as general-purpose processor device that includes registers and arithmetic/logic circuits, and*

executes a series of instructions to calculate a first and/or second hashing functions." Column 8, 65-67, Column 9, lines 1-3)

sending the first address to the first to N-th storage sections; *("The memory system 404 can include a first memory portion and a second memory portion. First memory portion 416 can include a number of entries that can be accessed according to address values generated by the first hash function calculator" Column 9, lines 7-10)*

when the second signal is received from the M-th (M is a natural number equal to or less than N) comparison section, storing the externally input data at the first address in the M-th storage section; *("The first memory portion 416 can include leaf entries with key and associated data information" Column 9, lines 20-21) ("A leaf pointer entry 106-2 can indicate that the system 100 holds exactly one key that hashes to the same bucket as the applied key value" Column 5, lines 28-31). The Examiner interprets the second signal as a signal that is sent when the input key matches, as in the case of the leaf-entry.*

when the second signal is not received from any of the first to N-th comparison sections and the third signal is received from one or more of the first to N-th comparison sections, storing the externally input key and data at the first address in the first storage section obtained when a storage section or storage sections that output the first signal among the

first to N-th storage sections are arranged in a first order; *("The first memory portion 416 can include...null entries like 420-3" Column 9, lines 20-23) ("In the event the data indicates a null value...a "no match" value is generated" Column 7, lines 24-25). The Examiner interprets the "no match" value as the third signal. The Examiner interprets the first order as the order that the memory of Greene's apparatus is arranged in.*

when the second signal is not received from any of the first to N-th comparison sections and the third signal is not received from any of the first to N-th comparison sections, sending the second address to the first to N-th storage sections; *("In the even no collision exists in the second store...a new chunk is built in a second store. In particular, pointers to key values and their associated data are written in chunk locations according to their corresponding second hashing function output values (step 320). Pointer information for the newly formed chunk is then written into the corresponding pointer...location in the first store (step 3222), thus completing the add of the new key to the system" Column 8, lines 34-42) The Examiner interprets the second signal not received as no collisions existing in the second store. The Examiner interprets that at step 308 of figure 3, that a null signal (third signal) was not received by the comparison sections of the first store.*

when the second signal is received from the L-th (L is a natural number equal to or less than N) comparison section, storing the externally input

data at the second address in the L-th storage section; *(Fig. 4, shows the second memory 418 storing the externally input data at the second address, as seen in the chunk 422. The second signal inherently must be received if the entry is a chunk pointer.)*

and when the second signal is not received from any of the first to N-th comparison sections and the third signal is received from one or more of the first to N-th comparison sections, storing the externally input key and data at the second address in the first storage section obtained when a storage section or storage sections that output the first signal among the first to N-th storage sections are arranged in a second order; (Second memory portion *("In the even no collision exists in the second store...a new chunk is built in a second store. In particular, pointers to key values and their associated data are written in chunk locations according to their corresponding second hashing function output values (step 320). Pointer information for the newly formed chunk is then written into the corresponding pointer...location in the first store (step 3222), thus completing the add of the new key to the system" Column 8, lines 34-42) The Examiner interprets the second signal not received as no collisions existing in the second store. The Examiner interprets that at step 308 of figure 3, that a null signal (third signal) was received by the comparison sections of the second store. The Examiner interprets the second order as the order that the memory of Greene's apparatus is arranged in.*

and a second processing section operating when data is read, the second processing section:

sending the first address to the first to N-th storage sections; and when the second signal is not received from any of the first to N-th comparison sections, sending the second address to the first to N-th storage sections.

The Examiner interprets the second processing section to possess all the limitations of the first processing section, except that the second processing section operates when data is read and not written. ("first memory portion 416 can be a random access memory (RAM). Second memory portion can also be a RAM. Further, the first and second memory portions may be different sections of the same RAM device" Column 9, lines 15-19). Because RAM may either read or write, it is inherent that the processor be capable of operating both when data is read or written.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harris C. Wang whose telephone number is 5712701462. The examiner can normally be reached on M-F 8-5:30, Alternate Fridays Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AYAZ R. SHEIKH can be reached on (571)272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HCW

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